REMARKS

In this Response to the above-identified Final Office Action, Applicants do not amend the application, but submit the following remarks and seeks reconsideration thereof. In this Response, no claims have been added, no claims have been cancelled, and no claims have been amended. Accordingly, Claims 1-22 are pending.

I. Claims Rejected Under 35 U.S.C. § 103(a)

Claims 1-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,935,247 issued to Pai *et al.* ("Pai") in view of the article "AGP Video System Memory Access" published by the PC Guide ("PC"). Applicants respectfully disagree for the following reasons.

With respect to claims 1, Applicants submit that neither Pai nor PC, separately or in combination, teaches or suggests a system memory including an isolated output area. Pai at most discloses a display buffer (FIG. 1) and a monitor driven by a video display card (col. 3, lines 61-63). PC at most discloses a video chipset sharing the system memory. Relying on the teaching of the two references, the Examiner arrives at a "combined memory" which includes a system memory (accessible by the video chipset) and a video memory (e.g., the display buffer) on a video card. The Examiner then characterizes the "combined memory" as the system memory, and the display buffer as the isolated output area. Applicants submit that the Examiner's reliance is misplaced, because a video memory on a video card cannot teach or suggest the system memory or a portion thereof. PC only mentions that the video card may share portions of the system memory, but in no way suggests that the video card is part of the system memory. It is known in the art of computer architecture that a video memory on a video card is both physically and logically distinguishable from a system memory. Physically, a video memory and a system memory are built by different technologies to accommodate different performance requirements (citing PC: "*The frame buffer requires the highest performance so it makes sense to leave it on the video card so special video-specific technologies like VRAM can be used.*"). Logically, a video memory on a

video card does not share the same address space as the system memory. PC explicitly discloses that frame buffer should be left on the video card. Thus, even though a portion of the system memory may be used for video purposes as disclosed by PC, the frame buffer remains on a separate video card. A processor cannot directly address the video memory on a separate video card, because a separate video card is part of a video subsystem having its own address space and memory management schemes for efficient graphics generation. Thus, the cited references in combination do not even remotely suggest the "combined memory" as proposed by the Examiner. Thus, Pai's display buffer (or frame buffer) characterized as isolated by the Examiner cannot teach or suggest the isolated output area included in the system memory as recited in claim 1.

Moreover, the combination of the two references is inapposite because the disclosure of PC explicitly teaches away the proposed combination. PC discloses that "*AGP is not the same as the ill-fated unified memory architecture (UMA). Under UMA, all of the video card's memory, including the frame buffer, is taken from main system memory.*" Thus, PC makes it clear that the frame buffer should not be part of the system memory. A frame buffer in the system memory would be limited by the performance of the system memory and would not be isolated from processes or devices that share access to the system memory. This point is further explained by the following passage of PC: "*The frame buffer requires the highest performance so it makes sense to leave it on the video card so special video-specific technologies like VRAM can be used.*" Thus, it is abundantly clear that PC teaches against using a system memory that includes a frame buffer. However, Applicants note that the Examiner, citing exactly the same passage, concludes that PC indeed allows a frame buffer and video memory to be system memory (page 4, end of second paragraph of the final office action). This conclusion ignores the clearing teaching of PC to separate the frame buffer from the system memory. Thus, the Examiner's conclusion is not supported by the cited reference.

Moreover, assuming for the sake of argument a person is to combine the two cited references to produce the "combined memory" as proposed by the Examiner. As the video memory and the system memory are technologically and logically different, there is no reasonable

expectation of success in combining them while maintaining the high performance and isolation of the frame buffer. The cited references recognize the difficulty and recommend the separation of the frame buffer from the system memory. Thus, the combination of the two references is inapposite for this additional reason.

For at least the reasons set forth above, Pai in view of PC does not render claim 1 obvious. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 1 are requested.

With respect to claims 2-22, Applicants note that these claims stand rejected under 35 U.S.C. § 103(a) over Pai only, because the Examiner does not cite PC in the rejection of these claims.

Claims 2-11 depend from claim 1 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to claim 1, Pai does not teach or suggest each of the elements of claims 2-11.

Moreover, with respect to claim 3, Pai in view of PC does not teach or suggest "the memory control hub (MCH) to permit the graphics card to access the isolated output area only when the graphics card is in isolated access mode" as recited in claim 3. In the rejection of claim 1, the Examiner has characterized the display buffer as the isolated output area and the graphics card as connecting to the monitor to drive the monitor output. The Examiner further characterizes the synchronization registers and the switch as the MCH. As shown in FIG. 3 cited by the Examiner, the MCH is not even connected directly or indirectly to the display buffer or the monitor. Thus, the MCH cannot possibly control the access to the display buffer by the graphics card. Thus, Pai does not teach or suggest each of the elements of claim 3 for this additional reason.

With respect to claim 4, the Examiner asserts that Pai discloses the claimed "wherein local storage of the data from the isolated output area is not permitted," because Pai teaches that the access of the stored genetic code is not permitted. Applicants note that the Examiner does not show how the access of the stored genetic code is related to the local storage of the data on the graphics card. Pai does not describe local storage of data on the graphics card or prohibiting doing so. Pai at most makes a passing reference to a graphics card in connection to driving the monitor

output. There is nothing in Pai that mentions whether local storage on the graphics card should or should not be permitted. Further, Pai also does not mention a direct memory access (DMA) controller on the graphics card. Thus, Pai does not teach or suggest each of the elements of claim 4 for this additional reason.

With respect to claim 8, the Examiner characterizes the OS nub as the software (col. 4, lines 49-57). However, as shown in FIG. 2 of Pai, the software is not the only entity that is permitted to write to the display buffer. The switch permits both software and hardware to write to the display buffer to form a complete text string containing the genetic code. This is in stark contrast to claim 8 reciting that the MCH only permits the OS nub (the software) to write to the isolated output area. Thus, Pai does not teach or suggest each of the elements of claim 8 for this additional reason.

With respect to claim 10, Pai does not teach or suggest a non-isolated bit plane, because Pai describes the display buffer and the graphics card as accessible only during the genetic code display procedure. The genetic code display procedure has been characterized by the Examiner as the isolated mode. Thus, Pai's graphics card and display buffer can at most contain isolated data. Thus, with the Examiner's characterization, under no circumstances does the graphics card contain non-isolated data. Furthermore, the concept of bit-plane is also missing in Pai's disclosure. The Examiner points to col. 5 lines 40-50 for teaching the bit-planes. However, the cited passage only described the access control to the display buffer. As the Examiner has already characterized the display buffer as the isolated output area in the system memory, where are the bit-planes in the graphics card? Thus, Pai does not teach or suggest each of the elements of claim 10 for this additional reason. Analogous discussion applies to claim 11. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 1-11 are requested.

With respect to claim 12, Applicants submit that Pai at least fails to teach or suggest an isolated execution environment and an isolated execution mode. The Examiner has characterized the genetic code memory and the display buffer as isolated. The genetic code memory and the display buffer are storage devices and thus do not "execute." The genetic code display procedure executed by the processor cannot possibly disclose the isolated execution mode, because there is no

indication as to how the processor would execute differently if the processor executes other procedures. The processor taught by Pai executes in the same execution mode for all procedures. Access restriction to input/output does not in any way indicate that there is a restriction or limitation on how the processor executes internally in different execution modes. Thus, Pai at least does not teach or suggest an isolated execution mode. Accordingly, reconsideration and withdrawal of the obviousness rejection of claim 12 are requested.

With respect to claim 17, Applicants resubmit the outstanding arguments from the prior responses, noting that the Examiner reasserts the same position in the Final Office Action without addressing Applicants' arguments. It appears that the Examiner has not considered the arguments previously submitted. Those arguments are reproduced below.

Applicants respectfully submit that Claim 17 depends on Claim 16, which in turn depends on Claim 13 following the dependency tree, one is able to discern that the windows occluded are all windows other than the window defined in the defining element of Claim 17, which is the window into which the isolated output area data from the bit plane on the graphics card is loaded. Stated differently, all non-isolated mode windows are occluded responsive to entry into the isolated mode. Accordingly, Applicants respectfully submit that the official notice of ATM machines, even if well taken, and even if it did render obvious, "to one of ordinary skill in the art [to] occlude the image prior to transitioning out of isolated execution mode, in order to preserve the security information being displayed," is inapposite here. Applicants respectfully submit that it is not the occlusion of information transitioning out of isolated execution mode that is being claimed. Rather, in Claim 17, the occlusion of other windows upon the entrance into isolated execution mode that is claimed. It is respectfully made for this additional reason, rejection of Claim 17 should be withdrawn.

With respect to claim 19, Applicants note that the claim stand rejected under 35 U.S.C. § 103(a) over Pai because only Pai is cited in this rejection. As discussed above, Pai does not teach or suggest a DMA controller or a MCH in connection with the isolated output area. Pai also fails to mention the interfaces coupled to the DMA controller. Accordingly, reconsideration and withdrawal of the obviousness rejection of claim 19 are requested.

Since all independent claims have been shown to be patentable over the reference of record, their dependent claims are at least patentable as dependent on a patentable independent claim. Accordingly, reconsideration and withdrawal of the obviousness rejection of all the dependent claims are also requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-22 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 13, 2005

Thomas M. Coester, Reg. No. 39,367

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF TRANSMISSION:

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on March 29, 2005.

Erin Flynn September 13, 2005